High Step-up Isolated DC-DC Converter with Multi-cell Diode-capacitor Network

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***Abstract*—The existing high step-up DC-DC converters with multi-cell diode-capacitor network have large inrush current issue and strict *LC* filter requirement which are not suitable to achieve both high efficiency and high power density in relatively low switching frequency and large power application. In order to meet high step-up voltage regulation and compulsory electrical isolation due to public safety, this paper proposes a single-switch isolated DC-DC converter which exploits the features of multi-winding transformer and diode-capacitor voltage boost cell. The new topology has the following advantages 1). increase voltage boost capability and avoid extreme large duty ratio. 2) achieve almost zero output voltage ripples which reducing the inductance in output *LC* filter, 3) reduce transformer turns ratio and magnetic component volume. Furthermore, it can use the transformer leakage inductor and auxiliary switch to achieve zero-voltage switching (ZVS), which is beneficial to reduce the switching loss and increase efficiency.**

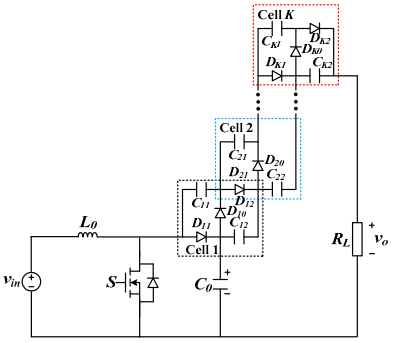
Keywords—Diode-capacitor network; high voltage gain; isolated DC-DC converter; multi-winding transformer; zero-voltage switching (ZVS)

I. INTRODUCTION

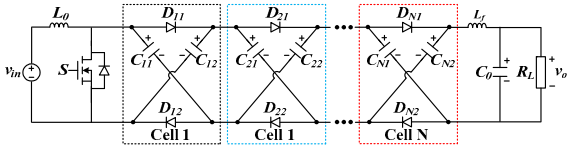
High step-up voltage boost capability is the basic requirement of power converter with wide input voltage range, high efficiency and high power density. It has been one of the key technical issues in solar and fuel cell generation system [1]-[4]. High voltage gain techniques mainly include isolated DC-DC converter with transformer, non-isolated DC-DC converter with couple inductor, multi-stages cascade structure, modular multilevel, switch-capacitor/inductor and impedance network. Compared with couple inductor and transformer, it is more suitable to achieve high efficiency and high power density using diode-capacitor network. A family of basic boost derived high step-up DC-DC converter introduces diode-capacitor network to achieve high voltage gain and avoid extreme large duty ratio. With increasing number of voltage boost cell, voltage gain can be further increased. Moreover, it does not increase the drive and control circuit complexity due to only one fully controllable switch. Compared to other existing techniques, high step-up DC-DC converter with diode-capacitor network is more promising in aforementioned medium and small power generation system.

Fig.1 shows two typical high step-up DC-DC converters with multi-cell diode capacitor network [5]. Fig 1(a) is widely used in low power supply chip such as LT3482, and it operates under f_s=1MHz. However, in aforementioned renewable energy generation, when f_s is not high enough, the directly energy charging and discharging between different capacitors causes large inrush current and increases switching loss significantly. For the circuit shown in Fig 1(b), besides the large inrush current issue, low pass filter is necessary due to pulsed DC voltage generated by diode-capacitor network [6]-[7]. In high voltage gain application, the amplitude of pulsed DC voltage is large and output current is relatively small, therefore the large inductance L_f is required to limit the output current and voltage ripples.

In order to overcome the drawbacks of inrush current and strict *LC* filter requirement, this paper propose a high step-up isolated DC-DC converter with multi-cell diode-capacitor network which exploits the advantages of multi-winding transformer and diode-capacitor voltage boost cell. It avoids inrush current issue and achieves almost zero output voltage ripples which are beneficial to the inductance in output *LC* filter. Meantime, it reduces transformer turns ratio and magnetic component volume which contributes to high power density. Furthermore, it can use the leakage inductor of transformer and auxiliary switch to realize zero-voltage switching of main switch (ZVS), which is beneficial to reduce



(a) Series connection of Multi-cell diode-capacitor network.



(b) Cascade connection of multi-cell diode-capacitor network.

Fig.1 High step-up DC-DC converters with multi-cell diode-capacitor network.

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the switching loss and increase efficiency. Section II describes the basic operation principle. Section III provides an active clamp main circuit to realize zero-voltage switching (ZVS) of the main switch and auxiliary switch. Finally, simulation results verify the theoretical analysis and advantages of the new topology.

II. Operation Principle of High Step-up Isolated DC-DC Converter with Multi-cell Diode-Capacitor Network

Fig.2 shows one of the basic voltage boost cell: two-port diode-capacitor network. When D_{11} and D_{12} are forward bias, C_{11} and C_{12} are connected in parallel and the terminal voltage meets:

$$v_2 = v_{C_{11}} = v_{C_{12}} = v_1 \tag{1}$$

When D_{11} and D_{12} are reversed blocked, C_{11} and C_{12} are connected in series and the terminal voltage meets:

$$v_2 = v_{C_{11}} + v_{C_{12}} - v_1 \tag{2}$$

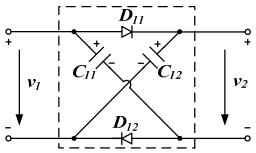


Fig.2 Basic diode-capacitor voltage boost cell.

Therefore, the *LC* filer is added in the output side to obtain the constant DC voltage.

Fig.3 shows the proposed high step-up isolated DC-DC converter with two-cell diode-capacitor network. The transformer can be equivalent as ideal transformer in parallel connection of magnetic inductor L_m and then in series connection of leakage inductor L_k. The first winding in the secondary side of transformer is connected to one two-port diode-capacitor cell in normal polarity and the second winding is connected to another two-port diode-capacitor cell in reversed polarity. The output of two diode-capacitor cells is connected in series to achieve high voltage gain with essential *LC* filter.

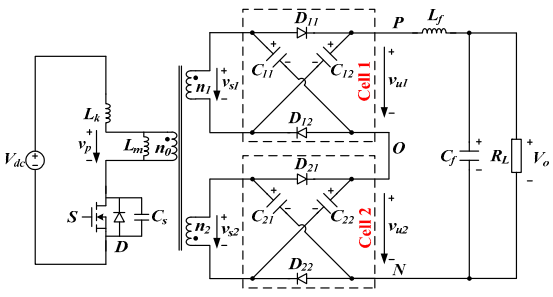


Fig.3 High step-up isolated DC-DC converter with two-cell diode-capacitor network.

For simple analysis, it is assumed that L_m is large enough (L_k<<L_m) and i_{Lm} is continuous conduction. The detailed operation principles are described as follows:

During *S*=ON interval, DC source charges the primary side of transformer. The magnetizing current i_{Lm} is increasing linearly by ignoring the influence of leakage inductance L_k. The transformer primary side voltage v_p and secondary side voltage v_{s1}, v_{s2} meets:

$$L_m \frac{di_{Lm}}{dt} = v_{p(S=ON)} \approx V_{dc} \tag{3}$$

$$v_{s1(S=ON)} \approx \frac{n_1}{n_0} V_{dc} \tag{4}$$

$$v_{s2(S=ON)} \approx -\frac{n_2}{n_0} V_{dc} \tag{5}$$

Where: n_0, n_1, n_2 are the turns ratio of transformer primary and secondary side windings, respectively.

The induced voltage v_{s1} is positive, and D_{11} and D_{12} are conducting, n_1 winding charges two capacitors C_{11} and C_{12} in parallel connection.

$$v_{u1(S=ON)} = V_{C11} = v_{s1(S=ON)} \tag{6}$$

The induced voltage v_{s2} is negative, and D_{21} and D_{22} are blocked, n_2 winding and two capacitors C_{11} and C_{12} are connected in series to supply the output capacitor.

$$v_{u2(S=ON)} = -v_{s2(S=ON)} + 2V_{C21} \tag{7}$$

During *S*=OFF interval, the energy stored in transformer is released through n_1 and n_2 windings. The induced voltage v_{s1} is negative, and D_{11}, D_{12} are blocked. n_1 winding and two capacitors C_{11}, C_{12} are connected in normal polarity to supply the output capacitor.

$$v_{u1(S=OFF)} = -v_{s1(S=OFF)} + 2V_{C11} \tag{8}$$

The induced voltage v_{s2} is positive, and D_{21}, D_{22} are conducting, n_2 winding charges two capacitors C_{21} and C_{21} in parallel connection. The winding terminal voltage v_{s2} is clamped by v_{C21}. The transformer primary, secondary voltage meets:

$$v_{u2(S=OFF)} = v_{s2(S=OFF)} = V_{C21} = V_{C22} \tag{9}$$

$$v_{p(S=OFF)} = -\frac{n_0}{n_2} V_{C21} \tag{10}$$

$$v_{s1(S=OFF)} = -\frac{n_1}{n_2} V_{C21} \tag{11}$$

In steady state, the average voltage across the magnetic inductor should be zero in one switching time period T_s. From (3) and (10), we have

$$DT_s \cdot v_{p(S=ON)} + (1-D)T_s \cdot v_{p(S=OFF)} = 0 \tag{12}$$

By solving the aforementioned equation, the voltage of the capacitor can be derived as

$$V_{C21} = \frac{n_2}{n_0} \cdot \frac{D}{1-D} V_{dc} \tag{13}$$

From (4), (5), (6), (7) and (13), during *S*=ON interval, the output voltage v_{pn} is:

$$v_{PN(S=ON)} = v_{u1(S=ON)} + v_{u2(S=ON)} = (\frac{n_1}{n_0} + \frac{n_2}{n_0} \cdot \frac{1+D}{1-D}) V_{dc} \tag{14}$$

From (8), (9), (11) and (13), during *S*=OFF interval, the output voltage v_{pn} is:

$$v_{PN(S=OFF)} = v_{u1(S=OFF)} + v_{u2(S=OFF)} = (\frac{n_1}{n_0} \cdot \frac{2-D}{1-D} + \frac{n_2}{n_0} \cdot \frac{D}{1-D}) V_{dc} \tag{15}$$

If two secondary windings have the same turns ratio $n_1 : n_0 = n_2 : n_0 = n$, during *S*=ON and *S*=OFF interval, v_{pn} has the same voltage and almost constant.

$$v_{PN} = \frac{2n}{1-D} \cdot V_{dc} \tag{16}$$

Therefore, two diode-capacitor cells in the secondary side operate in complementary mode to avoid inrush current and achieve almost zero output voltage ripples. L_f is designed to eliminate the switching noisy, and its value can be reduced to large extent. Furthermore, during both *S=ON* and *S=OFF* interval, transformer always provide energy to the output side. It is different from the transformer in conventional fly-back DC-DC converter, which needs relatively large air gap to store energy. Thus, it contributes to small volume.

In steady state, the voltage stress across *S* is reversed polarity connection of DC source and primary side winding during *S*=OFF interval. From (10) and (13), it can be derived as:

$$v_{S\_Mos} = V_{dc} - v_{p(S=OFF)} = \frac{1}{1-D} V_{dc} \tag{17}$$

All the diodes withstand the same voltage stress. The voltage across D_{11} and D_{12} during *S*=OFF interval is reversed polarity connection of v_{C11} and v_{s1}. From (4), (6) and (11), it can be derived as:

$$v_{S\_Diode} = v_{C11} - v_{s1(S=OFF)} = \frac{n}{1-D} V_{dc} \tag{18}$$

With increasing number of two-port diode-capacitor cells (*N=2k*), the voltage gain of high step-up DC-DC converter can be further increased. The main circuit is shown in Fig.4. Using similar derivation approach, the voltage gain, voltage stress of switch and diode can be rewritten as (19), (20) and (21).

$$G = \frac{v_o}{V_{dc}} = \frac{N \cdot n}{1-D} \tag{19}$$

$$v_{S\_Mos} = \frac{1}{1-D} V_{dc} = \frac{G}{N \cdot n} V_{dc} \tag{20}$$

$$v_{S\_Diode} = \frac{n}{1-D} V_{dc} = \frac{G}{N} V_{dc} \tag{21}$$

Where: *n* is transformer primary, secondary turns ratio, *N* is the number of diode-capacitor cell, *D* is duty ratio of *S*.

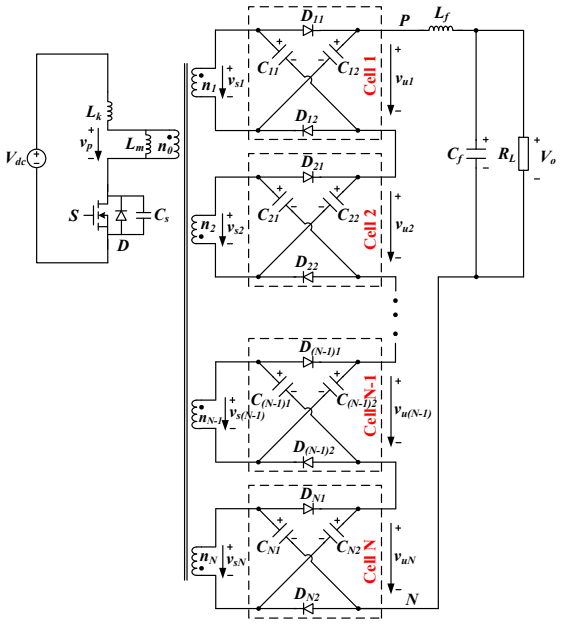


Fig.4 High step-up isolated DC-DC converter with multi-cell diode-capacitor network.

Fig.5 shows the relationships of voltage gain and boost duty ratio *D*, transformer turns ratio *n*, and number of basic diode-capacitor cells *N* for high step-up isolated DC-DC converter with multi-cell diode-capacitor network. Fig.6 and 7 show the voltage stress of switching device and power diode. With the increasing number of basic diode-capacitor cell, the voltage stress of switch device and power diodes can be further reduced.

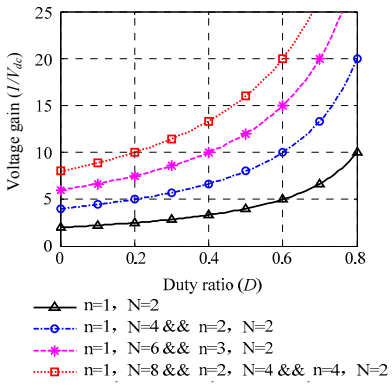


Fig.5 Voltage gain versus boost duty ratio.

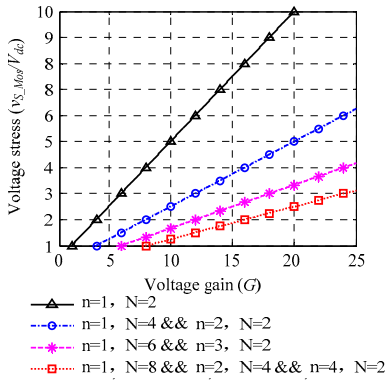


Fig.6 Voltage stress of switch.

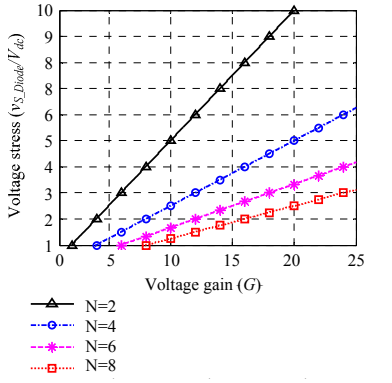


Fig.7 Voltage stress of power diodes.

III. ACTIVE CLAMPED CIRCUIT AND SOFT SWITCHING REALIZATION

The leakage inductor of transformer causes high voltage stress and spikes on the switching devices. In order to maintain power devices operating within the safe operating area (SOA), an active clamp circuit including auxiliary switch S_a and clamped capacitor C_r is introduced to absorb leakage energy. It suppresses voltage spikes as well as provides ZVS operation condition [8]-[10]. Fig.8 shows the active clamped high step-up isolated DC-DC converter with multi-cell diode-capacitor network (N=2). Assuming the converter operates under the continued current mode in steady state, Fig.9 shows the key steady state waveforms of different interval in one switching time period. It includes 8 operation modes in one switching time period.

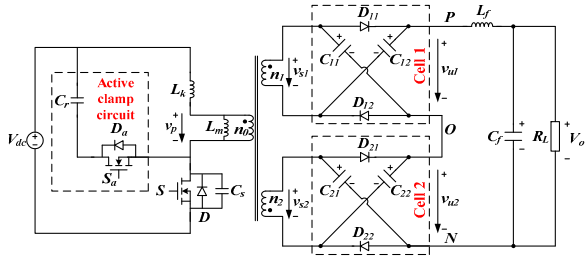


Fig.8 Active clamped high step-up DC-DC converter with multi-cell diode-capacitor network (N=2).

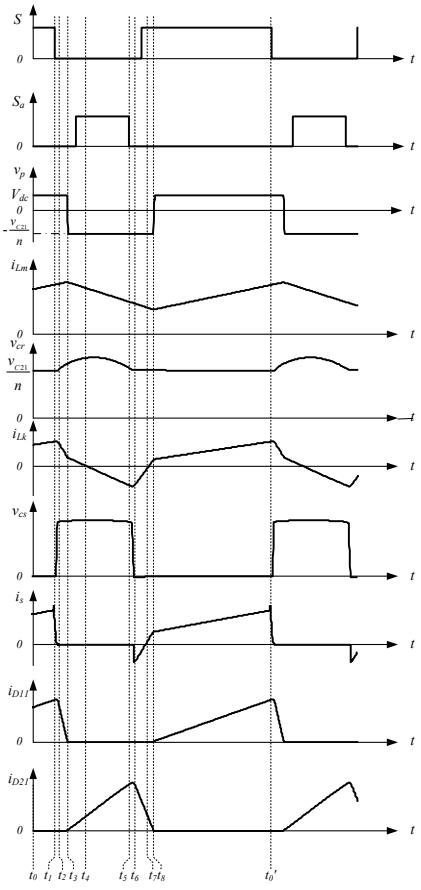


Fig.9 Operation principle of active clamped high step-up DC-DC converter with multi-cell diode-capacitor network (N=2).

Mode 1 (t_0-t_1): in this mode, S is always turned on, and S_a is turned off. The current across magnetic inductor L_m and leakage inductor L_k increase linearly, which can be expressed as:

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{v_{Lm}}{L_m} \cdot (t - t_0) \tag{22}$$

Where v_{Lm} can be approximately calculated as:

$$v_{Lm} = \frac{L_m}{L_m + L_k} V_{dc} \tag{23}$$

$$i_{Lk}(t) = i_{dc}(t) = i_{Lk}(t_0) + \frac{V_{dc} - v_{Lm}}{L_k} \cdot (t - t_0) \tag{24}$$

Mode 2 (t_1-t_2): at t_1 instant, S is turned off, and the energy stored in L_k is transferred to anti-parallel capacitor C_s of S. v_{Cs} increases immediately. Until t_2 instant, i_s decreases to zero, v_{Cs} increases from zero to V_{dc}+v_{Cr}. The voltage across main switch v_{DS} and leakage inductor current i_{Lk} are expressed as:

$$\begin{aligned} v_{DS}(t) &= v_{Cs}(t) \\ &= V_{dc}(1 - \cos(\omega_1 \cdot (t - t_1))) + i_{Lk}(t_1) \cdot Z_1 \cdot \sin(\omega_1 \cdot (t - t_1)) \end{aligned} \tag{25}$$

$$i_{Lk}(t) \approx i_{Lk}(t_1)\cos(\omega_1 \cdot (t - t_1)) + \frac{V_{dc} - v_{Cs}(t_1)}{Z_1} \cdot \sin(\omega_1 \cdot (t - t_1)) \tag{26}$$

Where: $\omega_1 = 1/\sqrt{C_s(L_m + L_k)}$, $Z_1 = \sqrt{(L_m + L_k)/C_s}$.

In practical application, the energy stored in C_s is far smaller than L_k. C_s charging process is very quick. Thus, the charging current of capacitor can be seemed as i_{Lk}.

$$v_{DS}(t) \approx \frac{i_{Lk}(t_1)}{C_s}(t - t_1) \tag{27}$$

The secondary winding v_{s1} charging C_{11} and C_{12} through D_{11} and D_{12}, C_{11} and C_{12} are connected in parallel to supply the output side. The secondary winding v_{s2} and C_{21}, C_{22} are in reversed polarity connection to supply the output side.

Mode 3 (t_2-t_3): at t_2 instant, the voltage across swich v_{DS} equals to V_{dc}+v_{Cr}. The anti-parallel diode of auxiliary switch D_a starts conducting, which suppress the turn off voltage spike across S. leakage inductor L_k and clamped capacitor C_r forms a resonant circuit. The charging current of C_r is:

$$i_{Cr}(t) = i_{Lk}(t) \approx i_{Lk}(t_2)\cos(\omega_2 \cdot (t - t_2)) + \frac{v_{Lk}(t_2)}{Z_2} \cdot \sin(\omega_2 \cdot (t - t_2)) \tag{28}$$

Where: $\omega_2 = 1/\sqrt{C_r(L_m + L_k)}$, $Z_2 = \sqrt{(L_m + L_k)/C_r}$.

D_{11} and D_{12} are still conducting, and the current start to decrease. The transformer primary side voltage is clamped. The voltage across L_m and L_k are expressed as (29) and (30), respectively.

$$v_{Lm}(t) \approx \frac{n_0}{n_1} v_{C11} \tag{29}$$

$$v_{Lk}(t) \approx -v_{Cr} - \frac{n_0}{n_1} v_{C11} \tag{30}$$

Therefore, i_{Lm} continues to increase and i_{Lk} starts to decrease.

In order to achieve ZVS of S_a, C_r should be selected to maintain half resonant period of L_k and C_r is large than the S=OFF interval in one switching time period T_s. Thus, C_r needs to meet:

$$C_r \geq \frac{(1 - D_{\min})^2}{\pi^2 L_k f_s^2} \tag{31}$$

Where: D_{min} is the minimum on-state duty ratio of S, L_k is leakage inductance and f_s is witching frequency.

Mode 4 (t_3-t_4): at t_3 instant, i_{D11} and i_{D12} decrease to zero and D_{11}, D_{12} are reversed biased. The leakage inductor current suppresses the reverse recovery issue of power diode. D_{21}, D_{22} starts to conduct, the primary side voltage v_p is reversed and clamped by v_{s2}. i_{Lm} achieves the maximum value. The commutation of powe switch S and diodes in the secondary side are completed. v_{Lm} and v_{Lk} meet:

$$v_{Lm}(t) \approx -\frac{n_0}{n_2} v_{C21} \tag{32}$$

$$v_{Lk}(t) \approx -v_{Cr} + \frac{n_0}{n_2} v_{C21} \tag{33}$$

Therefore, after t_3 instant, i_{Lm} starts to decrease and i_{Lk} continues to decrease. In order to achieve ZVS of S_a, S_a should be trigged on before t_4 instant, when i_{Lk} is reversed.

Mode 5 (t_4-t_5): at t_4 instant, the current of auxiliary switch i_{sa} is reversed. D_a is blocked, and S_a starts to conduct. S_a realizes ZVS. D_{11} and D_{12} are blocked. The secondary winding v_{s1} and C_{11}, C_{12} are in reversed polarity connection to supply the output side. D_{21} and D_{22} are conducting. The secondary winding v_{s2} and C_{21}, C_{22} are in parallel connection to supply the output side.

Mode 6 (t_5-t_6): at t_5 instant, S_a is turned off. D_a is blocked. L_k, DC source, transformer primary side and C_s forms new resonant circuit. C_s is very small, thus C_s discharges quickly by i_{LK}. Until t_6 instant, v_{Cs} decreases to zero. v_{Cs} can be expressed as:

$$v_{Cs}(t) \approx v_d - (v_d - v_{Cs}(t_5))\cos(\omega_3(t - t_5)) + i_{Lk}(t_5)Z_3 \sin(\omega_3(t - t_5)) \tag{34}$$

Where:

$$v_d = V_{dc} + \frac{n_0}{n_2} v_{C21},\ \omega_3 = 1/\sqrt{C_s(L_k + L_m)},\ Z_3 = \sqrt{(L_k + L_m)/C_s}.$$

In order to achieve ZVS of S, the energy of L_k should be larger then that of capacitor C_s. So, L_k meets:

$$L_k > \frac{C_s v_{Cs}^2(t_5)}{i_{Lk}^2(t_5)} \tag{35}$$

Mode 7 (t_6-t_7): at t_6 instant, C_s discharges to zero. The anti-parallel diode of switch D starts to conduct. Before i_{Lk} is reversed, S should be triggered on.

Mode 8 (t_7-t_8): before t_7, S is triggered on, and it achieves ZVS. At t_7 instant, i_{Lk} is reversed. D_{21} and D_{22} are still conducting, and i_{D21}, i_{D22} decrease. The transformer primary side voltage v_p is clamped, v_{Lm} and v_{Lk} are expressed as (36) and (37), respectively. i_{Lm} continues to decrease and i_{Lk} increases linearly.

$$v_{Lm}(t) \approx -\frac{n_0}{n_2} v_{C21} \tag{36}$$

$$v_{Lk}(t) \approx V_{dc} + \frac{n_0}{n_2} v_{C21} \tag{37}$$

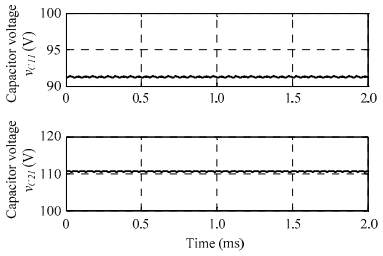
At t_8 instant, i_{D21} and i_{D22} decrease to zero, and they are reversed biased. D_{11} and D_{12} start to conduct. The transformer secondary side voltage v_{s1} is clamped to v_{C11}. i_{Lm} achieves minimum value. The commutation of switch S and diodes in the secondary is completed. Until t_0' instant, S is triggered OFF, and the circuit enters into a new switching time period.

IV. Simulation Verification

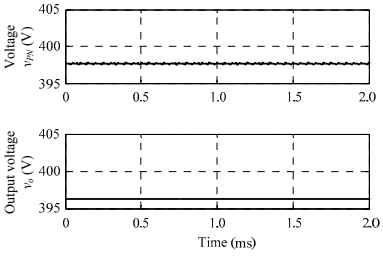
Numerical simulations using MATLAB/Simulink have been performed to verify the proposed topology and operation principles. The main circuit parameters are: V_{dc}=30~48V, V_o=400V, L_k=10uH, L_m=400uH, C_r=4.7uF, C_s=1.5uF, C_{11}=C_{12}=C_{21}=C_{22}=200uF, L_f=5uH, C_f=250uF, R_{Load}=320Ω, T_s=50us。

Fig.10 shows the waveforms for high step-up isolated DC-DC converter with multi-cell diode-capacitor network (N=2) when d=0.55. It includes the transformer current i_{Lk}, i_{Lm}, switching voltage v_S, v_{Sa} and current i_S, i_{Sa}, and the intermediate capacitor voltage v_{C11}, v_{C21}, the output voltage before and after filtered v_{PN}, v_o. The measured capacitor voltage v_{C11}=v_{C12}= 92V, v_{C21}=v_{C22}=112V shown in Fig.9 (a) is a little smaller than the theoretical value 96V and 116V due to voltage drop of transformer leakage inductor and power devices. As shown in Fig.9 (d) and (e), the maximum voltage across S and S_a is clamped within 140V when they are turned off, thus the relatively low voltage MPSFET can be used. Before S and S_a are turned on, the drain source voltage decrease to zero. Thus, both switches achieve ZVS.

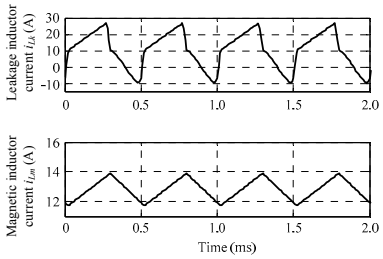
Fig.11 shows the corresponding waveforms for high step-up isolated DC-DC converter with multi-cell diode-capacitor network (N=2) when V_{dc}=30V. In steady state, d=0.72. The simulation results are almost consistent with the theoretical calculated value. S and S_a achieve ZVS under wide input voltage range.



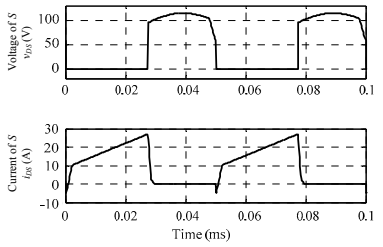
(a) Capacitor voltage of C_{11} and C_{21}.



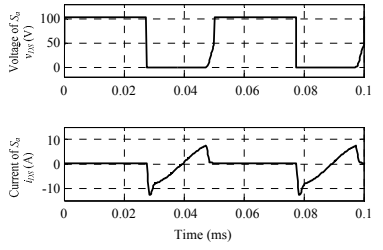
(b) v_{PN} and filtered output voltage v_o.



(c) i_{Lk} and i_{Lm}.

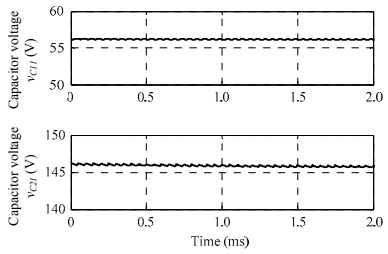


(d) Voltage and current of S.

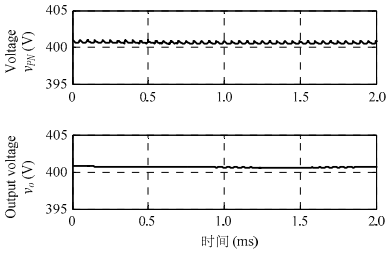


(e) Voltage and current of S_a.

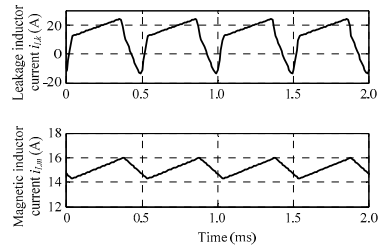
Fig.10 Waveforms of active clamped high step-up DC-DC converter with multi-cell diode-capacitor network (N=2).



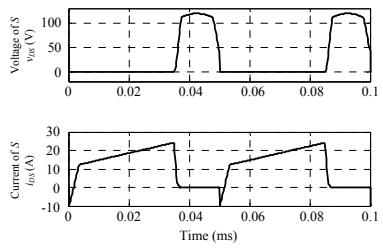
(a) Capacitor voltage of C_{11} and C_{12}.



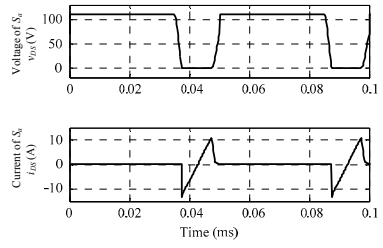
(b) v_{Pn} and filtered output voltage v_o.



(c) i_{Lk} and i_{LM}.



(d) Voltage and current of S.



(e) Voltage and current of S_a.

Fig.11 Waveforms of active clamped high step-up isolated DC-DC converter with multi-cell diode-capacitor network (V_{dc}=30V, d_{son}=0.72).

V. CONCLUSION

The existing high step-up DC-DC converters with multi-cell diode-capacitor network have inrush current issue and strict *LC* filter requirement which is not suitable to achieve high efficiency and high power density in relatively low switching frequency and large power application. In order to overcome these drawbacks, this paper proposes a new topology of high step-up isolated DC-DC converter with multi-cell diode-capacitor network which exploits the features and advantages of multi-winding transformer and diode-capacitor network. It avoids inrush current issue and achieves almost zero output voltage ripples which reducing the inductance in output *LC* filter. Meantime, the reduced transformer turns ratio and magnetic component volume contributes to high power density. Furthermore, new topology can use the leakage inductor of transformer and auxiliary switch to realize ZVS, which is beneficial to reduce the switching loss and increase efficiency. With improved performance, the new topology is more promising in solar and fuel cell generation system where high step-up voltage boost capability is one of the key requirements in wide input range voltage regulation.

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